Code No: V0421/R07

SET - 1

II B.Tech II Semester, Regular Examinations, Apr – 2011

PULSE AND DIGITAL CIRCUITS

(Com. to ECE, BME, ECC)

Time: 3 hours Max Marks: 80

Answer any FIVE Questions

All Questions carry equal marks

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1. a) Verify that one of the levels of the voltage across Capacitor $V_2 = (V/2)\ (e^{2x}-1) / (e^{2x}+1) = (V/2) \tan hx$ when a symmetrical square wave with time period of 'T' is applied to a low pass RC circuit. Here $x = T/(4RC)$.
   b) A 1 kHz symmetrical square wave of ±10 V is applied to an RC circuit having 1 ms time constant. Calculate and plot the output for the RC configuration as i) high-pass circuit ii) Low pass circuit.

2. a) Explain transfer characteristics of the emitter coupled clipper and derive the necessary equations.
   b) Draw the basic circuit diagram of positive peak clamper circuit and explain its operation.

3. Write the following in detail:
   a) Diode switching times, b) Switching characteristics of a transistor and c) FET as a switch.

4. a) With the aid of circuit diagram, obtain the mathematical relation that a collector coupled astable multivibrator can function as a voltage to frequency converter.
   b) Consider a symmetrical collector coupled astable multivibrator using n-p-n Si transistors. The circuit and device parameters are: $V_{CC} = 6$ V, $R_C = 560\ \Omega$, $R = 5.6$ k Ω, $C = 50$ pF, $h_{FE} = 40$ and $r'_{bb} = 100\ \Omega$. Calculate i) the waveforms at the base and collector of one transistor and plot to the scale. Also find the recovery time and frequency of oscillations.

5. a) Draw and explain the typical waveform of a time-base voltage generator. Explain various types of errors encountered in time base generators.
   b) Explain the principle of working of exponential sweep circuit with neat circuit diagram and also derive the equations for slope, transmission and displacement error.

6. a) How an astable multivibrator can be synchronized? Illustrate with waveforms.
   b) A symmetrical astable multivibrator using Germanium transistors and operating from a 10 V collector supply voltage has a free period of 1ms. Triggering pulses whose spacing is 750 µs are applied to one base through a small capacitor from a high impedance source. Find the minimum triggering pulse amplitude required to achieve 1:1 synchronization. Assume that the timing portion of the base waveform is linear.

7. a) Sketch circuit of a simple diode bidirectional sampling gate and describe its functioning with neat waveforms. Obtain the expressions for gain A, and the two minimum control voltage levels.
   b) Describe the operation of chopper amplifier. Give the operation of the transistor as a chopper switch in ON state and in OFF state.

8. a) Realize a two input TTL NAND gate truth table and explain its operation with suitable circuit diagram.
   b) With the help of neat circuit diagram and truth table, explain the working of diode logic AND gate, and RTL AND gate.

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1. a) Prove that an RC low pass circuit behaves like an integrator if RC>15T, where T is the time period of the input sinusoidal signal.
   b) A 10 Hz square wave is applied to an RC high pass circuit. Calculate and draw the output waveform voltage levels under the following conditions: The lower 3-dB frequency is i) 0.3 Hz ii) 3 Hz iii) 30 Hz.

2. a) Explain the operation of a clamping circuit whose output signal has negative offset. What modifications are needed if the output voltage of the clamper circuit has positive offset?
   b) Design a diode clamper circuit to restore the positive peaks of 1 kHz input signal to a voltage level equal to 5V. Assume that the diode voltage during forward bias condition is 0.7 V.

3. a) Define rise time, storage time, fall time, and turn off time in the case of transistor as a switch.
   b) Design a common emitter transistor switch operating with two power supplies V_{CC} = 18 V, -V_{BB} = -12 V. The transistor is expected to operate at I_C = 8 mA, and I_B = 0.75 mA. The static current gain is 25. Assume Si transistor, and $R_2 = 5R_1$.

4. a) Draw the self biased symmetrical binary circuit and derive the necessary relations for steady state analysis of the circuit.
   b) Discuss about different triggering methods used in multivibrator circuits.

5. a) What are the methods available for generating time-base waveforms? Explain the operation of one of them.
   b) Design a relaxation oscillator to have 2 kHz output frequency using UJT for the given specifications: Supply voltage: 20 V, Intrinsic stand off ratio: 0.70, Peak Current = 2 µA, Valley current: 1mA, and V_v = 3V. Assume necessary data.

6. a) What do you mean by synchronization?
   b) What is the condition to be met for pulse synchronization?
   c) Compare sine wave synchronization with pulse synchronization.

7. a) With neat diagrams, explain the principle of operation of four diode bidirectional sampling gate. Compare the performance of the circuit with that of six diode bidirectional sampling gate.
   b) Describe the errors encountered in series sampling and what is the design procedure that is adopted to minimize these errors.

8. a) With the help of neat circuit diagram and truth table, explain the working of a three input DTL NAND gate.
   b) What do you mean by 'fan in' and 'fan out'? Discuss about the DTL NAND gate circuit which can improve Fan out of the gate.

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SET - 3

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1. a) Derive the expression for percentage tilt (P) of a square wave output of RC high pass circuit.
   b) An ideal 1 μs pulse is fed to a low pass circuit. Calculate and plot the output waveform under the following conditions: the upper 3-dB frequency is i) 10 MHz ii) 0.1 MHz iii) 0.01 MHz.

2. a) Draw a circuit diagram for getting a slicing the input sinusoidal signal to 2V on either side of the signal. Assume that the amplitude of the applied signal is more than ±2V.
   b) Draw the transfer characteristics of double ended clipping circuit and explain its operation with suitable circuit diagram.

3. a) A rectangular pulse of voltage is applied to the base of a transistor driving it from cutoff to saturation. Discuss the changes in the output potential. Explain the various times involved in the switching process.
   b) Design a transistor circuit that acts as switch for the given specifications: V_{CC} = 20 V, I_C = 5 mA. It is a 'Si' transistor having h_{FEmin} = 20. Assume necessary data.

4. a) Explain the operation of an emitter bistable multivibrator circuit with suitable sketches.
   b) Design a Schmitt trigger circuit to have UTP = 6 V, LTP = 3 V using silicon transistors whose $h_{FE(min)}$ = 40. Assume necessary data.

5. a) With the help of suitable sketches, explain the working of constant current sweep generator.
   b) Design a transistor ramp generator to provide an output amplitude of 12V over a time period of 2 ms. The input signal is a negative going pulse with an amplitude of 5 V, a pulse width of 2ms and the time interval between pulses is 0.5 ms. The total load resistance is 2 k ohms and the ramp is to be linear within 1%. The supply is to be ±15 V, and h_{FEmin} = 50. Assume necessary data.

6. a) Illustrate the terms 'Synchronization' and 'frequency division' of a sweep generator.
   b) A free running relaxation oscillator has sweep amplitude of 100 V and a period of 1 ms synchronizing pulses are applied to the device such that breakdown voltage is lowered by 50 V at each pulse. The synchronizing pulse frequency is 4 kHz. What is the amplitude and frequency of synchronized oscillator waveform?

7. a) Illustrate with neat circuit diagram, the operation of unidirectional sampling gate for multiple inputs.
   b) Explain the operation of a two input sampling gate which does not have any loading effect on control signal.
   c) Give the importance of chopper amplifier.

8. Explain the following:
   a) Realization of AND, and OR gates using universal gates.
   b) What do you mean by 'fan in' and 'fan out'? Discuss about the DTL NAND gate circuit which can improve 'fan out' of the gate.

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1. a) Derive suitable expression for output voltage of an RC high pass circuit if an exponential input is applied as an input.
   b) A 10 Hz symmetrical square wave whose peak to peak amplitude of 2 V is applied to a high pass RC circuit whose lower 3-dB frequency is 5 Hz. Calculate and sketch the output waveform for the first two cycles. What is the peak – to – peak output amplitude under steady state conditions?

2. a) Draw the circuit diagram of slicer circuit using Zener diodes and explain its operation with the help of its transfer characteristic.
   b) Draw the circuit diagram of emitter coupled clipper. Draw its transfer characteristics indicating all intercepts, slopes and voltage levels derive the necessary equations.

3. a) Describe the sequence of events that lead to reverse recovery time, storage time, and transition time in a semiconductor diode.
   b) A common emitter circuit with Si transistor has V_{CC} = 15 V, R_C = 15 k ohms, and I_B = 0.3 mA. Determine the value of $h_{FE(min)}$ for saturation to occur. If R_C is changed to 500 ohms, will the transistor be saturated?

4. a) Explain the operation of an emitter coupled monostable multivibrator circuit.
   b) Design a collector coupled monostable multivibrator circuit for the given specifications: V_{CC} = 8V, V_{BE} = -1.5V, $I_{C(sat)}$ = 2 mA, period of the quasi stable state is 2.0 μs. $h_{FE(min)}$ = 20, the ON transistor (Si) has base current which is 50% in excess of minimum base current. Assume $R_2 = 2R_1$, and I_{CBO} = 0. Assume suitable data.

5. a) Explain the basic principles of the Miller and Bootstrap time base generators with suitable sketches.
   b) Obtain expression for slope error in the case of a constant current sweep circuit.

6. a) Explain the factors which influence the stability of a relaxation divider with the help of neat waveforms.
   b) A UJT sweep operates with Vv = 3V, Vp=16V and η = 0.5. A sinusoidal synchronizing voltage of 2V peak is applied between bases and the natural frequency of the sweep is 1kHz, over what range of sync signal frequency will the sweep remain in 1:1 synchronism with the sync signal?

7. a) What is sampling gate? Explain how it differs from Logic gates?
   b) What is pedestal? How it effect the output of sampling gates?
   c) What are the drawbacks of two diode sampling gate?

8. a) Why totem pole is used in DTL? Draw the circuit diagram and explain a DTL gate with this.
   b) Verify the truth table of a two input RTL-NOR gate with the circuit diagram and explain its operation.